IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: PETROLLI, Jean Paul

SERIAL NO.: (International Serial No. PCT/FR2005/000529)

FILED: Herewith (International Filing Date: 7 March 2005)

TITLE: PROGRAMMABLE LOGIC ARRAY FOR SCHEDULE-CONTROLLED PROCESSING

REMARKS ON PRELIMINARY AMENDMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

In conjunction with the filing of the present application, and prior to an initial Official Action on this matter, please amend the above-identified application as provided in the attached Marked Up Copy and Substitute Specification.

Please note that the following amendments in the Substitute Specification apply to the attached specification and claims labeled for "U.S. filing". This combined application incorporates the original application and any amendments or annex to the International Application in the proper order, including the correct original and substitute pages, claims and drawing sheets.

In this preliminary amendment, please consider the following remarks in conjunction with the amendments to the above-identified application as follows:

REMARKS

The present Preliminary Amendment has been entered for the purpose of placing the application into a more proper U.S. format. In particular, certain grammatical and idiomatic inconsistencies have been corrected by amendment to the specification, and the application is

corrected for certain typographical errors found in the originally submitted application. No new matter has been added by these amendments. The present application incorporates the original filing including any amendments made in the international filing. There was no amendment in the International Application, and there is no annex to the International Preliminary Examination Report because a Demand for an IPER was not filed.. The present specification is an English language translation of an originally French language document.

The Claims have been amended so as to conform with U.S. requirements and so as to remove multiple dependent claims. The Abstract has been amended so as to conform to U.S. filing requirements.

Applicant respectfully requests that the present Amendment be entered prior to an initial Official Action on the present application.

Respectfully submitted,

7-10-06

Date

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CLAIMS

I claim:

1. (Currently amended) Electronic circuit of data processing to emulate a logic function~~. This~~ , the circuit ~~is characterized the following elements~~ comprising:

a single clock providing representative signals of a time unit~~;~~;

a synchronous programmable logic array processing values per time unit~~;~~;

a means of state change detection, ~~designated "events" of~~ designating events as internal or external values~~;~~;

a means of programming signals for changing state or directly programming the events~~;~~ ; and

a means of successive scheduled times processing providing~~; to the~~ a logic array~~;~~ with representative scheduled time signals according to the signals provided by the means of state change detection or by the means of programming ~~of events and the~~ signals or the events ~~provided by the clock~~, the processing mean being adapted to determine scheduled times, at time delay~~ed~~s by programming ~~by~~ the programming mean~~; to happen~~s, a function to happen being provided with signals by the ~~said~~ means of detection ~~of the said mean of programming;~~

~~the~~; wherein processed operations done by the logic array ~~being the~~ result ~~of~~ from successive scheduled times initiated by internal or external state changes~~;~~ and ~~by~~ a successive scheduled time determination.

2. (Currently amended) Electronic circuit according to the claim 1, ~~characterized by the fact that~~ wherein the logic array reproduces ~~the~~ a simulator operation ~~has the possibility to be~~ integrated

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into an electronic circuit, ~~the~~ a clock defining time unit being tuned for ~~the~~ reproduction of the simulator.

3. (Currently amended) Electronic circuit according to the claim 1, ~~characterized by the fact that~~ wherein the logic array is able to emulate, at real time, a logic function without any logic element emulation.

4. (Currently amended) Electronic circuit according to ~~any of claim 1 to 3, characterized by the fact that~~ Claim 1, wherein the logic array ~~consists~~ is comprised of internal logic processing cells and peripheral communication cells with the outside of the electronic circuit, the signals provided by the scheduled time processing controlling the operation through at least one internal cell or one peripheral cell.

5. (Currently amended) Electronic circuit according the claim 4, ~~characterized by the fact that~~ wherein the cells exchange data through one single group of lines on which is set up an exchange per time unit, the cells being adapted to generate signals, random or programmed events, towards the scheduled time processing unit, the ~~said~~ means of processing scheduled time providing to each cell a command group.

6. (Currently amended) Electronic circuit according to ~~any of claims 1, 4 or 5, characterized by the fact that~~ Claim 4, wherein the cells of internal processing cells are able to process a logic word per time unit.

7. (Currently amended) Electronic circuit according to claim 6, ~~characterized by the fact that~~ wherein the internal logic cells are adapted to merge several data group issued of several respective identities and to memorize each merged logic word.

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8. (Currently amended) Electronic circuit according to ~~claims 4 to 7, characterized by the fact that~~ Claim 4, wherein the peripheral cells are adapted to sample logic words received from the external of the circuit and to generate merged logic words according the communication direction.

9. (Currently amended) Electronic circuit according to the claim 5, ~~characterized by the fact that~~ wherein the logic array ~~consists~~ is comprised of a specific means of communication with the outside of the circuit, the logic array setting up memorized logic words adapted to be read or modified by the ~~said~~ specific communication mean.

10. (Currently amended) Simulator~~, characterized by the fact that it consists of~~ comprising:

an electronic circuit according to ~~any one of claims 1 to 9~~ Claim 1.

11. (Currently amended) Emulator~~, characterized by the fact that it consists of~~ comprising:

an electronic circuit according to ~~any one of claims 1 to 9~~ Claim 1.

12. (Currently amended) Electronic circuit according the claim 4, ~~characterized by the fact that~~ further comprising:

a scheduler ~~which needs~~ needing no scheduled time processing other than delays managed by a register matrix and a conflict detection between scheduled times.

13. (Currently amended) Electronic circuit according the claim 12, ~~characterized by the fact that~~ wherein the specific communication means reads and changes ~~reading and changing of~~ scheduled times ~~by the said specific communication mean~~.

14. (Currently amended) Electronic circuit according the claim 4, ~~characterized by~~ further comprising:

a logic combination of output datas formed of internal or peripheral communication cells.

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ABSTRACT OF THE DISCLOSURE

The electronic data processing circuit targets the emulation of a logic function. The circuit ~~comprises~~ includes a single clock providing time unit signals, a programmable synchronous logic array for processing values on a time unit basis, ~~a means for detecting~~ detection of internal or external value state changes known as events , ~~a means for programming~~ programmer for state changes or event signals, ~~a means for processing~~ processor for a series of scheduled times providing the logic array with scheduled time signals depending on the signals from the detection ~~means~~ or the event ~~programming means~~ programmer and the signals from the clock~~, wherein said processing means~~. The processor can determine subsequent scheduled times having delayed deadlines programmed by the ~~programming means~~ programmer, depending on the signals from ~~said~~ the detection ~~means~~ or ~~said~~ the programmer ~~programming means~~. The processing performed by the logic array is thus dependent on the series of scheduled times triggered by internal or external value state changes and by determination of the series of scheduled times.

Substitute Specification

CLAIMS

I claim:

1. (Currently amended) Electronic circuit of data processing to emulate a logic function, the circuit comprising:

a single clock providing representative signals of a time unit;

a synchronous programmable logic array processing values per time unit;

a means of state change detection, designating events as internal or external values;

a means of programming signals for changing state or directly programming the events; and

a means of successive scheduled times processing providing a logic array with representative scheduled time signals according to the signals provided by the means of state change detection or by the means of programming signals or the events, the processing mean being adapted to determine scheduled times, at time delays by programming the programming means, a function to happen being provided with signals by the means of detection; wherein processed operations done by the logic array result from successive scheduled times initiated by internal or external state changes and a successive scheduled time determination.

2. (Currently amended) Electronic circuit according to the claim 1, wherein the logic array reproduces a simulator operation integrated into an electronic circuit, a clock defining time unit being tuned for reproduction of the simulator.

3. (Currently amended) Electronic circuit according to the claim 1, wherein the logic array is able to emulate, at real time, a logic function without any logic element emulation.

4. (Currently amended) Electronic circuit according to Claim 1, wherein the logic array is comprised of internal logic processing cells and peripheral communication cells with the outside of the electronic circuit, the signals provided by the scheduled time processing controlling the operation through at least one internal cell or one peripheral cell.

5. (Currently amended) Electronic circuit according the claim 4, wherein the cells exchange data through one single group of lines on which is set up an exchange per time unit, the cells being adapted to generate signals, random or programmed events, towards the scheduled time processing unit, the means of processing scheduled time providing to each cell a command group.

6. (Currently amended) Electronic circuit according to Claim 4, wherein the cells of internal processing cells are able to process a logic word per time unit.

7. (Currently amended) Electronic circuit according to claim 6, wherein the internal logic cells are adapted to merge several data group issued of several respective identities and to memorize each merged logic word.

8. (Currently amended) Electronic circuit according to Claim 4, wherein the peripheral cells are adapted to sample logic words received from the external of the circuit and to generate merged logic words according the communication direction.

9. (Currently amended) Electronic circuit according to the claim 5, wherein the logic array is comprised of a specific means of communication with the outside of the circuit, the logic array setting up memorized logic words adapted to be read or modified by the specific communication mean.

Substitute Specification

10. (Currently amended) Simulator comprising:

an electronic circuit according to Claim 1.

11. (Currently amended) Emulator comprising:

an electronic circuit according to Claim 1.

12. (Currently amended) Electronic circuit according the claim 4, further comprising:

a scheduler needing no scheduled time processing other than delays managed by a register matrix and a conflict detection between scheduled times.

13. (Currently amended) Electronic circuit according the claim 12, wherein the specific communication means reads and changes scheduled times.

14. (Currently amended) Electronic circuit according the claim 4, further comprising:

a logic combination of output datas formed of internal or peripheral communication cells.